Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)
Office Action Summary		09/458,121	MOAS ET AL.
		Examiner	Art Unit
		Tuan A. Vu	2193

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>27 December 2005</u>.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1,3-11,13-20 and 22-25</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1,3-11,13-20 and 22-25</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date <u>20050321</u>.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   This action is responsive to the Applicant's response filed 12/27/05.

As indicated in Applicant's response, claims 1-2, 4-11, 13-20, and 22-25 have been

amended. Claims 1-2, 4-11,13-20, and 22-25 are pending in the office action.

Claim Objections

2.   Claims 4-5, 10-11, 13-15, 19-20, 22-23 are objected to because of the following

informalities.

Claims 4-5, 13-14, and 22-23 recites 'the availability of resources ... <u>are</u> determined ...';

and the 'are' needs to be corrected to match with the singular of 'the availability'.

Claims 10 and 19 recites 'according to requirements of the multiple ... in the <u>bock</u> of

code' (line 9, 11, respectively); and the typographical error in 'bock' needs to be corrected.

Claim 19 recites 'a first set of instructions ... generat<u>e</u>...' and 'a second set of instructions

... caus<u>e</u>...' (first 5 lines). The verbs 'generate' and 'cause' need to be corrected to match with

the singular of 'a ... set of instructions'.

Claims 11 and 20 recite '... cause said processor to perform said method further

comprising:' (line 3) while claims 15 and 23 recite 'additional instructions... cause the processor

to perform the method further comprising:' (lines 1-3). The clause recited as 'to perform

...<u>method further comprising</u>:' appears awkward; and needs to be corrected to say, for example,

'to further perform the steps comprising:'

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4.   Claims 1-2, 5, 10-11, 14, 19-20, and 22 are rejected under 35 U.S.C. 102(b) as being

anticipated by Long et al., USPN: 5,835,958 (hereinafter Long) .

As per claim 1, Long discloses a method comprising:

inserting a single instruction at a start of a block of code (step 204 – Fig. 2a; *wrapper* -

col. 5, lines 8-17 – Note: a call to a stack-checking function reads on a single instruction) to

determine if resources of a processor are available for the block of code, wherein the block of

code includes multiple instructions (step 206 – Fig. 2A – Note: a function being called reads on

multiple instructions); and

if the resources are available, modifying the available resources (e.g. Fig. 2A; col. 5, lines

18-28; col. 6, line 64 to col. 7, line 28; *trampoline function* - col. 7, line 66 to col. 8, line 27)

according to requirements of the instructions in the block of code.

As per claim 2, Long discloses determining a set of available resources that will be

available after said block of code has executed (e.g. Fig. 4; *epilogue ... new stack chunk to be*

executed.. re-lock... reflector frame – col. 9, lines 10-20; col. 10, lines 15-21).

As per claim 5, Long discloses availability determined at runtime (Fig. 2A-B – Note:

usage and manipulation of data already stored in a stack reads on dynamic process).

As per claim 10, Long discloses a computer-readable medium having stored thereon a set of instructions to monitor processor resources (e.g. Fig. 5), said set of instruction, which when executed by a processor, cause said processor to perform a method comprising:

inserting (a single instruction at a start of ... to determine if resources of a processor are available for the block of code... includes multiple instructions); and

if the resources are available, modifying (the available resources ... requirements of the instructions .. block of code)

All of these limitations have been addressed in claim 1; hence this claim is rejected based on the corresponding rationale as set forth therein.

As per claims 11 and 14, these claims are the computer-readable medium or apparatus claims corresponding to method claims 2 and 5, respectively, hence are rejected herein with the same reasons as set forth above.

As per claim 19, Benson discloses a computer readable medium having a first set of instructions (e.g. Fig. 5), which when executed, generate a second set of instructions through a binary translation process, the second set of instructions (e.g. Fig. 2A-B – Note: verifying code invocation reads on second set of instructions) when executed cause the processor to perform a method comprising the steps of:

inserting (a single instruction at a start of ... to determine if resources of a processor are available for the block of code... includes multiple instructions); and

if the resources are available, modifying (the available resources ... requirements of the instructions .. block of code)

All of these limitations have been addressed in claim 1; hence this claim is rejected based on the corresponding rationale as set forth therein.

As per claims 20 and 22, this claim corresponds to claim 2 and 5; hence is rejected with the corresponding rejection as set forth therein.

Claim Rejections - 35 USC § 103

5.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6.   Claims 4, 6-9, 13, 15-18, and 23-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Long et al., USPN: 5,835,958, and further in view of Yellin et al., USPN: 5,740,441(hereinafter Yellin).

As per claim 4, Long does not explicitly disclose the availability of the processor resources is determined at a-compile time; but Long teach pre-execution stack-oriented verifying method that is desired to grow dynamically on a as-needed basis in an platform-independent software execution environment (see col. 1, line 50 to col. 2, line 31). Yellin, in a method to execute Java bytecodes which is analogous to the platform independent stack-based endeavor by Long, discloses verifier code (see *jsr() call, SnapShot data, program Verifier*) for checking stack data and a class loader for a interpreter/compiler Java runtime machine in which bytescode are interpreted or dynamically translated for execution (e.g. Fig. 4a-c; *compiled into bytecodes* - col. 12, line 61 to col. 13, line 59). In view of the desirability by Long to have a method using stack-based checking in a platform-independent runtime environment, it would have been obvious for

one of ordinary skill in the art at the time the invention was made to provide Long with Yellin's

pre-execution verification engine so that it perform the stack resources checking in a Java

interpreter/compiler (as taught by Yellin). Based on the well-known concept of a Just-in-Time

compiler similar to Yellin's stack-based pre-runtime method, one would be motivated to do the

modification to Long because it would provide Long with the platform flexibility and possibility

to obviate unnecessary recompiling as desired by Long dynamic stack growing method, which is

shown via Yellin's stack-based verification process working on the multi-platform portable

bytecodes.

As per claim 6, Long does not disclose signaling an error message if the resources of the

processor needed for the block of code are not available; and in response to the error message

branching to a fault handler routine. But in view of the limited resources on a given architecture

stack, memory availability is not unlimited; and according to a network connected runtime

execution by Long, when memory conflict occurs, an exception as a error to alert the system

would be suggested (see memory allocation errors - col. 10, line 48 to col. 10, line 6). Based on

the Java interpreter/compiler by Yellin, memory violation at runtime can be thrown as a message

to be handled via exception handler (e.g. Yellin: Appendix 1, col. 14 lines 58-65; step *440* Fig.

4B; step *454* Fig. 4C). In view of the bytecodes inter-platform operability and interpreter Java

engine over network connected machines and the rationale as set forth in claim 4, it would have

been obvious for one of ordinary skill in the art at the time the invention was made to provide

Long with error handling message as taught by Yellin during execution of network bytecodes

when certain memory resources are conflicting with the demand of the running code, when all

the dynamic allocation have been exhausted because only via exception being thrown (i.e. as a

error message) as above shown by Yellin would Long's runtime environment be prevented from incurring more memory catastrophic failures.

As per claim 7, this claim subject matter falls under the ambit of error message and handler by a processor to handle the memory conflict exception in claim 6; hence is rejected using the rationale as set forth therein.

As per claim 8, there is no explicit teaching by Long on a bit vector. However, Yellin discloses the stack resources are represented by a bit vector (col. 7, lines 25-55) while stack memory by Long is managed and observed for allocation as chunks via a *stack chunk context structure* that indicates how stack resources are being used (Fig. 2; *stack reflector* - col. 7, line 9-65). Arranging a structure of stack chunk to reflect the usage condition of the stack resources by Long can be viewed as a vector indicating status of stack chunk usage as purported by Yellin. In case the target code by Long is a bytecodes for an interpreter in a Java runtime environment as shown by Yellin (see TABLE 1, TABLE 2 col. 15-21) as set forth via the rationale of claim 4, it would have been obvious for one of ordinary skill in the art at the time the invention was made to make the stack chunk structure by Long so that it is implemented as a JSR bit vector as by Yellin, because of the JSR bit vector is a Java code handy to be use to support the snapshot of the stack resources as purported by Yellin, and this is exactly what the stack reflector process used by Long is intended to do; making the bit vector in Java useful because the JSR call is written in the very same code as the target language.

As per claim 9, Yellin disclose a JSR call at pre-execution of a bytecode hence Long combined with Yellin by virtue of claim 8, disclose wherein said bit vector is generated dynamically.

As per claims 13, 15-18, these claims are the computer-readable medium or apparatus

claims corresponding to method claims 4, 6-9, respectively, hence are rejected herein with the

same reasons as set forth above.

As per claims 23-25, these claims are the computer-readable medium or apparatus

claims corresponding to method claims 6-8, respectively, hence are rejected herein with the same

reasons as set forth above.

Response to Arguments

7.   Applicant's arguments filed 12/27/2005 have been fully considered but they are mostly

moot in view of the new grounds of rejection.

However, on pg. 10 of the Applicant's Remarks, Applicants have submitted that Yellin

does not disclose 'modifying available resources ... block of code'. The argument against Yellin

does not take into consideration why Yellin has been used in the 103 type of rejection as set forth

above; and appears to have attacked Yellin as if Yellin were taken alone to anticipate one

specific limitation; when fact the teaching by Yellin has been specifically used to address some

limitations that are viewed obvious in light of the base reference (not the limitations that are

already addressed by the base reference). In response to applicant's arguments against the

references individually, one cannot show nonobviousness by attacking references individually

where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413,

208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir.
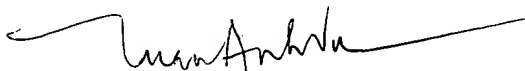
1986).

Conclusion

8.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tuan A Vu whose telephone number is (272) 272-3735. The

examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kakali Chaki can be reached on (571)272-3719.

The fax phone number for the organization where this application or proceeding is

assigned is (571) 273-3735 (for non-official correspondence – please consult Examiner before

using) or 571-273-8300 (for official correspondence) or redirected to customer service at 571-

272-3609.

Any inquiry of a general nature or relating to the status of this application should be

directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan A Vu
Patent Examiner,
Art Unit 2193
February 13, 2005